

Applications and technological evolution of FinFET in modern technology

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Abstract. FinFET technology, hailed as the successor to MOSFETs, has garnered significant attention due to its potential to address the challenges posed by the latter's scaling limitations. However, the adoption of FinFETs is not without its set of obstacles. Key issues, such as constraints imposed by material-induced bandgaps, the intricacies of manufacturing processes, and complications related to fin height, persistently challenge engineers and researchers alike. Notably, the material-induced bandgap limitations can be detrimental to the device's overall performance. The intricacies in manufacturing add layers of complexity to fabrication, making the production process not only meticulous but also expensive. Additionally, the precise control over fin height is crucial, as it has direct implications for device performance and variability. In response to these challenges, innovative solutions are continually being proposed. The advent of multiple gate designs has offered greater control over the device's electrical properties. Additionally, the integration of High-K dielectrics provides an improved gate oxide alternative, addressing the leakage current issues often observed in traditional designs. Moreover, techniques like selective epitaxial silicon growth have been introduced to rectify the external surface, ensuring better consistency and performance. Undoubtedly, these hurdles underscore the importance of relentless research and collaboration in the semiconductor industry. The drive to overcome these challenges not only pushes the boundaries of FinFET technology but also promises enhanced performance, efficiency, and scalability. This continuous evolution will undoubtedly pave the way for more refined and efficient FinFET solutions in the near future.

Keywords: Challenges, Fabrication, Materials, Improvements, Characteristics.

1. Introduction

As chip and system complexities surge, designing integrated circuits becomes an increasingly daunting task. Traditional MOSFET technology faces limitations, particularly in terms of low reliability and excessive leakage. Enter FinFETs, a groundbreaking solution to these challenges. With their unique architecture, which involves multiple gates that shield the drain potential from the channel, FinFETs effectively address the shortcomings of MOSFETs. These transistors offer tangible benefits such as enhanced power, performance scalability, and superior control over short-channel effects. This transformative shift in transistor technology has undeniably reshaped the semiconductor landscape.

While there's a wealth of literature discussing FinFETs, many focus on specific areas like corner effects, quantum phenomena, double patterning, and layout dependencies. Such studies often emphasize

layout and shape perspectives. However, this particular article offers a different vantage point, delving into materials, fabrication, and other pertinent factors.

The central aim here is to shed light on the latest advancements in FinFET technology and its evolution. This article embarks on a swift theoretical exposition of FinFETs, touching upon foundational technology, operational principles, and defining characteristics. From there, it transitions to a practical analysis, probing into the intricacies of design rules, short-channel effects, and reliability concerns. The challenges plaguing FinFETs are then elucidated, coupled with proposed innovative solutions geared towards optimizing performance, minimizing leakage, and boosting efficiency. The narrative culminates by underscoring the boundless potential of FinFET technology and the pivotal role of collective effort within the semiconductor sector to fully harness its capabilities.

2. Theoretical Analysis

2.1. FinFET and Its Core Technology

"Finned field effect transistor" (abbreviated as "FinFET") is a transistor technology utilized in the production of semiconductors. Due to the three-dimensional, fin-like structure of FinFETs, the channel may be controlled more effectively, enhancing both performance and energy efficiency.

A multigate device, a MOSFET constructed on a substrate with the gate positioned on two, three, or four sides of the channel or wrapped around the channel, is a fin field-effect transistor [1]. FinFETs with thick oxide on top of the fin are known as double-gate FinFETs [2]. The excess silicon can be accounted for in the design by using hyperbolic silicon layers, which significantly lowers the electric field from the gate to the fin [3]. FinFETs having thin oxide coatings on the sides and top of the fin are known as tri-gate FinFETs. To boost packing density, transistors can be placed closer together, and the height of the fins can be raised to improve energy efficiency [4].

In conclusion, FinFETs represent a substantial development in transistor technology, delivering greater performance characteristics, improved control, and lower leakage, especially in advanced semiconductor processes. The foundation of FinFET technology is the three-dimensional multigate architecture, making it a major force in contemporary semiconductor production.

2.2. Working Principle and Characteristics of FinFET

2.2.1. Working principle. Three-Dimensional Structure: A FinFET, or fin field-effect transistor, is a form of transistor that uses a three-dimensional fin-like structure, which is composed of a thin silicon fin that is vertically positioned on the substrate. The performance of transistors is improved and the channel is better controlled by this configuration.

Gate All Around (GAA): FinFETs contain a gate that encloses the fin on three sides (gate-all-around), enabling enhanced electrostatic control over the channel [5]. The standard planar MOSFET has the gate on the top surface, in contrast to this gate-all-around design.

Control of Gate Voltage: By supplying a gate voltage, the electrostatic field regulates the flow of current through the fin between the source and drain terminals, turning on or off the transistor. The channel can be controlled more effectively due to the three-dimensional structure, which also lowers leakage current in the off state [6].

Better Electrostatic Control: The front and rear gates of the multigate architecture provide better electrostatic control over the channel, overcoming issues brought on by shorter channel lengths. This function is essential for controlling power usage and enhancing efficiency.

Short-Channel Effects Mitigation: As transistors are shrunk to lower dimensions, short-channel effects are a major worry that the three-dimensional design helps address.

2.2.2. Characteristics. Energy Efficiency: FinFETs are renowned for their increased energy efficiency, which is one of their main advantages. Less power is consumed as a result of decreased leakage current

and improved electrostatic control. This energy efficiency is especially important in contemporary semiconductor technologies, where reducing power consumption is an important design factor.

Adapting to Smaller Nodes: FinFET technology allows semiconductor devices to be scaled down to smaller technology nodes (like 10nm, 7nm, etc.). The three-dimensional fin structure improves performance and scalability at advanced nodes by overcoming issues caused by the downsizing of conventional planar transistors.

Lessened Leakage Current: FinFETs' capacity to reduce leakage current problems brought on by reduced transistor sizes is one of its main advantages. By reducing leakage routes, the three-dimensional structure improves total energy efficiency by lowering off-state leakage currents.

Use of High-K dielectric: FinFETs frequently employ high-k dielectric materials in the gate construction to further improve performance, lowering current leakage and raising overall effectiveness [7].

Greater Threshold Voltage Control: FinFETs offer greater threshold voltage control, which is essential for the exact switching of the transistor. The dependability of digital circuits is increased and static power consumption is reduced as a result of this improved control. Improving the transistor's performance during the switch between the on and off states.

Use in Logic and SRAM Circuits: The use of FinFET technology in SRAM and logic circuits is mentioned in the document. For optimizing power consumption in various circuit settings, specific modes, such as short gate (SG) mode and low power (LP) mode, are described [8].

In conclusion, FinFETs perform better than conventional planar transistors. FinFETs have enhanced control and performance due to their operation on the basis of a three-dimensional multigate structure. FinFETs are a vital component of contemporary semiconductor production due to their emphasis on minimizing short-channel effects, lowering leakage, and utilizing cutting-edge materials. This has led to the creation of smaller, quicker, and more power-efficient electronic devices.

3. Current Research Analysis

According to research on FinFET materials, structure, and manufacturing methods, FinFET has numerous benefits over MOS as an alternative material.

First, do material research. For low power, the research emphasizes the need of field-effect transistors (FETs) having "typically off" properties. As a result, the Gold gate metal hafnium oxide combination has a higher ION/IOFF Ratio than Aluminium. The use of an insulator FinFET structure, as well as totally depleted nMOS and pMOS FinFETs, has been shown. Furthermore, this exhibited FinFETs with fin widths as small as 5nm and fin heights as tall as 65nm [9]. A material of 300mm SOI wafers with buried SiO₂ of 145nm and crystalline SiO₂ of 65nm is employed.

Second, in terms of structure, this article introduces two types of FinFET structures, dual-gate and tri-gate structures, as well as their production techniques and advantages [10]. It offers us an understanding of the benefits of FinFETs, such as lower power consumption and increased performance.

Third, in terms of fabrication and advantages, the paper introduces FinFET, a self-aligned double-gate MOSFET with scalability down to 20 nm that is aimed to overcome difficulties in sub-50-nm MOSFETs. In terms of layout and fabrication, FinFET is similar to its root, the conventional MOSFET. As a gate material, boron-doped SiGe is used in the fabrication process. The method yields gate lengths as short as 17 nm. The FinFET has self-aligned gates for the source and drain, which reduces parasitic capacitance and resistance while enabling control over the channel length. The experimental results show that FinFETs are effective at suppressing short-channel effects. Furthermore, the paper discusses device properties for various gate lengths, such as current-voltage characteristics and subthreshold leakage. The importance of gate engineering in managing the threshold voltage of ultrathin SOI-MOSFETs is emphasized. The usage of SiGe with a mole fraction of 60% Ge as a gate material is discussed.

These essential aspects demonstrate the evolution, properties, and benefits of FinFET as a promising nano CMOS device.

4. Challenges

FinFET technology, while transformative in the realm of semiconductors, grapples with a set of inherent challenges. One salient concern arises from the short channel length, which potentially compromises the device's performance due to quick channel effects. Additionally, when delving into III-V semiconductors such as In-GaAs, the smaller band gaps compared to silicon lead to elevated band-to-band tunneling currents.

Another point of contention is the High Electron Mobility Transistor (HEMT) devices. Their performance can be negatively impacted by the gate leakage current and support current problems they face. As FinFETs venture into smaller nodes, the looming shadows of reliability issues, including negative-bias temperature instability (NBTI) and hot carrier injection (HCI), can jeopardize the long-term stability of these devices. This is reminiscent of the challenges standard bulk MOSFETs face, particularly with concerns like concentration punch-through that diminish current quality and drive capability. Moreover, the intricate process of crafting FinFETs, especially those with double gates, is a step above the manufacturing complexity of traditional transistors. While their superiority in performance, control, and reduced leakage is undeniable, consistency in fin height and precise control during production becomes paramount. The ever-present specter of process unpredictability is exacerbated when crafting smaller nodes, making uniformity a Herculean task given the sensitivities to variations in size, composition, and doping levels.

FinFETs' three-dimensional architecture presents unique thermal challenges. As they shrink in size and power densities soar, managing heat dissipation is paramount. Financially, the advanced design, materials, and intricate manufacturing process elevate their production costs. Thus, the industry faces a delicate dance between enhancing performance and maintaining cost-effectiveness. The onus is on the semiconductor realm to foster continuous research, innovation, and partnership, ensuring FinFET technology's unwavering advancement.

5. Improvement Measures

Several innovative strategies have been proposed to address the challenges associated with FinFET technology. One significant approach involves the design of multiple gate transistors. The introduction of FinFETs mitigates short channel effects and offers enhanced control over device performance. Furthermore, the utilization of high-k dielectrics becomes indispensable for boosting performance in nanoscale dimensions by reducing undesired current flow.

An interesting proposal is the incorporation of a dual-KK structure in FinFETs. This design targets uneven drain extensions, aiming to elevate efficiency and refine metrics such as transconductance, output conductance, and cutoff frequency. Emphasizing material optimization, there's a push towards refining the In-GaAs-on-Insulator material, especially for gates with increased length and width. This requires meticulous planning around source and drain spacings.

Hafnium oxide, when combined with a gold gate metal, stands out for its potential to raise the ION/IOFF ratio while curbing leakage current. Another noteworthy strategy is the use of selective epitaxial Si growth, aimed at enhancing FinFET performance by mending the fin's exterior surface.

Thermal challenges inherent to FinFETs demand innovative thermal management solutions. This might necessitate the exploration of novel materials or advanced cooling techniques. With the reliability of FinFETs in focus, addressing issues like hot carrier injection and negative-bias temperature instability becomes paramount. Delving into cutting-edge transistor materials and designs can be a potential solution. Economic considerations also come into play, emphasizing the need for cost-efficiency in production processes. Striking a balance between cost and performance improvements is crucial. Lastly, achieving precise and consistent doping in the fin warrants the development of enhanced doping methods, ensuring uniform transistor properties. Overall, these enhancements aim to revolutionize FinFET technology, promising superior performance, reduced leakage, and heightened efficiency. However, it's essential to remember that specific metrics might vary based on the application and context of FinFET devices.

6. Conclusion

The paper delves into the advent of FinFETs as a promising solution in the realm of semiconductor technology. It elucidates the operating mechanisms and the foundational aspects of FinFET technology, highlighting its unique three-dimensional multi-gate architecture. This design not only bolsters performance and control but also significantly curtails leakage issues. The three-dimensional configuration, coupled with a full-gate design, renders the FinFET highly energy-efficient. Furthermore, its adaptability to smaller nodes, minimized leakage, and suitability for logic circuits set it apart in its functional domain. Nevertheless, the trajectory of FinFET innovation isn't devoid of challenges. Beyond the quick channeling effects, material limitations, reliability concerns, and manufacturing intricacies mentioned, there lie additional hurdles. These encompass thermal constraints, process variability, and financial considerations. The road ahead for researchers and industry experts involves untangling these complications. Potential avenues for progress include the development of advanced multi-gate transistors, harnessing high-k dielectrics, refining material choices, and devising effective thermal management strategies. In essence, this article sheds light on the evolution, challenges, and prospective advancements of FinFET technology within the semiconductor sector. It underscores the imperative of continuous research, collaboration, and ingenuity to navigate challenges and augment FinFET's capabilities, ultimately aiming to enhance efficiency and performance.

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